REMARKS

Claims 1 - 4 and 6 - 15 remain active in this application. Claim 13 has been amended to overcome the Examiner's objection under 35 U.S.C.§112. Support for the amendment of the claim is found throughout the application, and particularly shown in Figures 2 and 3. Claim 6 has been amended to clarify the subject matter contained therein. Support for this amendment is found throughout the application, and particularly shown in Figure 1. No new matter has been introduced into the application.

The Examiner has objected to claims 13-15 as failing to comply with the written description requirement and being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention under 35 U.S.C. §112. This objection is respectfully traversed as being moot in view of the amendment to claims 13 which revises the claim syntax to clarify the points raised by the Examiner in accordance with the Examiner's observations. The possible construction on which this ground of rejection is based was not intended and is believed to by precluded by the above amendment. Accordingly, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Although withdrawal of the previous grounds of rejection of claims 1-12 under 35 U.S.C. §101, 102 and 112 is noted, it is now noted that the rejection of claims 1-12 are made under 35 U.S.C. §102 as being anticipated by U.S. Patent 5,740,391 to Hunt (hereinafter "Hunt"). It is further noted that claims 3-4 have been newly rejected under 35 U.S.C. §103 as being unpatentable over Hunt. These grounds of rejection are respectfully traversed for the reasons of record, and in view of the amendments above and remarks below.

To summarize, the present invention is directed to an instruction buffer and a method for controlling an instruction buffer, particularly for a processor having a pipelined architecture such that several instructions can be processed simultaneously, either in-order or out-of-order. For this purpose, the invention includes two (parallel) instruction registers in which different and mutually exclusive classes of instructions may be stored in order of priority of execution and

through which dependencies (e.g. where the execution of one instruction must be deferred until the completion of another instruction) and readiness for execution may be expressed, preferably through a validity bit and dependence and release control fields (68, 69, 88, 89). Thus, the instruction registers 22, 23 of the invention can function to deliver instructions in-order or out-of-order in accordance with dependencies while the respective buffers function in a first-in-first-out (FIFO) age-sensitive manner to prevent the instruction buffer(s) from becoming filled with instructions awaiting execution, which slows overall processing.

In sharp contrast therewith, Hunt teaches a system and method that minimizes additional logic required to track early exception conditions in a microprocessor system, as well as eliminating premature false signaling of exceptions (see column 3, lines 35-54, in Hunt). While Hunt appears to provide separate but serially connected buffer units (342, 344 in Figure 3 in Hunt), and may preclude a parallel path/pipeline for out-of-order execution, the instruction buffer 316 functions as a single first-in-first-out (FIFO) buffer where retire unit 322 removes instructions from the instruction buffer 316 in program order (see column 7, lines 38-46, and Figures 3 and 4 in Hunt). In other words, Hunt specifically teaches that although instructions are sorted between an ALU instruction buffer 410 and a memory access buffer 420, the instructions are still "retied" in a FIFO manner (see column 7, lines 54-57, and Figure 4 in Hunt). Furthermore, the function of the claimed subject matter and its organization is very different from that of Hunt where Hunt fails to teach or contemplate any difference in order of instructions in the single instruction buffer. Hunt only teaches the insertion of instructions into the single instruction buffer 316 and removal from the same buffer in the same order of entry (see column 7, lines 47-54, in Hunt) for the purpose of preventing premature exception signaling when the buffer management unit 328 encounters a mispredicted branch instruction.

With regard to claim 1 of the present invention, Hunt clearly does not answer the recitation of first and second buffers wherein each issues instructions in storage entry order. Therefore, it is respectfully submitted that Hunt does not anticipate claim 1, nor dependent claims 2-4, of the present invention and the ground of rejection based on Hunt under 35 U.S.C. §102 is untenable in regard to the claims. It is also respectfully submitted that Hunt fails to make

obvious the subject matter contained in claims 3-4 to one of ordinary skill in the art and the ground of rejection based on Hunt under 35 U.S.C. §103 is untenable in regard to the claims. As previously discussed, if the single FIFO buffer/pipeline is necessary to maintain program order for instruction retirement, addition of a parallel path with out-of-order instructions would be inconsistent therewith. Thus, the proposed modification of Hunt would be improper under *In re Gordon*, 221 U.S.P.Q. 1125 (1984), since operation in the intended manner would be precluded. Accordingly, it is respectfully requested that the grounds of rejection based on Hunt with regard to claims 1-4 be reconsidered and withdrawn.

With regard to claims 6-10 of the present invention, claim 6 has been amended to emphasize that while one instruction in the second group of instructions is executed, other instructions in the first group of instructions are contemporaneously executed. Hunt clearly fails to teach or suggest such a method for controlling a buffer queue where instructions in two different groups are contemporaneously executed. Therefore, it is respectfully submitted that Hunt does not anticipate claim 6, nor dependent claims 7-10, of the present invention and the ground of rejection based on Hunt under 35 U.S.C. §102 is untenable in regard to the claims.

With regard to claims 11-15 of the present invention, Hunt clearly teaches only <u>one instruction buffer and one order</u> for instructions issued (see column 7, lines 41-42, in Hunt - "...the retire unit 322 *must* remove instructions from the instruction buffer 316 *in program order*.") (emphasis added). Furthermore, the instructions in Hunt are merely sorted between the ALU instruction buffer 410 and the memory access buffer 420, but are still "retied" in FIFO manner (see column 7, lines 54-57, and Figure 4 in Hunt). Therefore, it is respectfully submitted that Hunt does not anticipate claim 11, nor dependent claims 12-15, of the present invention and the ground of rejection based on Hunt under 35 U.S.C. §102 is untenable in regard to the claims. Accordingly, it is respectfully requested that the ground of rejection based on Hunt with regard to claims 11-15 be reconsidered and withdrawn and the application be passed to issue.

For the aforementioned reasons, it is respectfully submitted that Hunt does not anticipate any claim in the application and the ground of rejection based on Hunt is untenable in regard to the claims as not amended. In addition, it is respectfully pointed out that the Examiner has not

made a *prima facie* demonstration of anticipation of the subject matter contained in claims 1-4 and 6-15. Accordingly, it is respectfully requested that the ground of rejection based on Hunt be reconsidered and withdrawn and the application be passed to issue.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,

Marshall M. Curtis
Reg. No. 33,138

Whitham, Curtis & Christofferson, P. C.
11491 Sunset Hills Road, Suite 340
Reston, Virginia 20190

Customer Number: **30743**

(703) 787-9400